Holistic Energy Management with µProcessor Co-Optimization in Fully Integrated Battery-less IoTs

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***Abstract*—Fully integrating on-chip power management modules and microprocessor into a system-on-a-chip (SoC) provides many benefits including lower cost and higher levels of optimization, especially for battery-less energy harvesting operation. However, previous studies have only focused on optimization of individual module, e.g. power converter. There is a lack of systematic optimization of energy efficiency considering microprocessor, regulator, and harvester. This paper performs a holistic study on power efficiency of the whole energy harvesting system including solar cells, on-chip voltage regulators and microprocessors. An optimal scheduling and operation strategy is proposed for achieving the best efficiency and system level performance while avoiding local minimum as in conventional approach. We show that the minimum energy point is different from conventional approaches without a holistic view of the system. We demonstrated the study and proposed scheme using a battery-less solar energy harvesting system and a 65nm fully integrated test chip with 20% additional energy savings.**

Keywords— Low-power design; Power/energy/thermal aware architecture design; Multi-domain power/energy management

I. INTRODUCTION

Low power devices used for the Internet-of-Things (IoT) have become one of the fastest growing consumer markets. According to a survey from Cisco, the number of devices has surpassed the human population and has sustained an exponential growth rate since 2007. It is projected that by 2020 there will be 50 billon connected devices, i.e. 6.5 device per person on earth [1]. Smart, connected devices have spread across almost all commercial and industrial sectors including healthcare, manufacturing, agriculture and automobiles [2]. However, IoT devices still face several critical challenges that slow broad adaptation, mainly (1) device costs and (2) battery lifetime [3]. Highly integrated systems with reduced device count and cost has led to the popularity of system-on-chip (SoC) solutions that integrate regulators, ADC, microcontrollers [4, 5]. The majority of IoT devices rely on battery power, leading to high maintenance costs, limited operation time, and high ecological costs. Recently, energy harvesting, battery-less operation has emerged as a way to reduce these negative impacts. However, the energy volatility of the harvesting environment brings new challenges to modern low power electronics such as requirement for energy tracking, power adaptation and uncertainty in power supply. Because of these challenges, this paper focuses on holistic optimization of a fully integrated system running in an energy harvesting environment.

Tremendous efforts have been spent on developing fully integrated on-chip power management system along with microprocessors [6-10]. Deploying on-chip regulators brings significant benefits to low power electronics, including (1) lower device area and Bill-of-material (BOM) costs; (2) better overall system operation efficiency due to the flexibility of DVFS for each on-chip modules; (3) holistic optimization opportunities where system efficiency is further improved beyond the local optimization of individual modules.

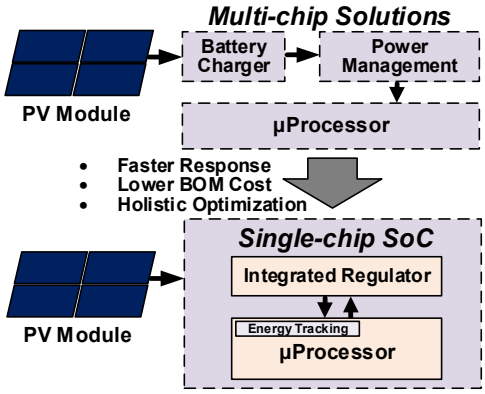

Fig. 1. System configuration of battery-less fully integrated energy harvesting SoC in comparison with conventional multi-module solution.

Most existing analysis on energy harvesting systems only considers either power management circuitry or high level system dynamics, but do not perform optimization across circuit stacks, e.g. energy source, regulators, microprocessors. For instance, an active maximum power point tracking (MPPT) circuit is used to modulate power converter frequency so that the energy harvester stays at its maximum power point voltage [11]. An efficient ultra-low power fully integrated voltage doubler was designed with only 3nW idle power and deliver 3uW output power [12]. A direct conversion mode was proposed to be added to avoid large conversion ratio between battery and load [13]. At the system level, researchers try to preserve memory consistency and forward progress of computation in the face of abrupt and intermittent power failures. Techniques for federating energy storage have been used to reduce power failures [15]. Rewriting application code into energy-aligned tasks ensures forward progress on computation despite failure [16]. Adapting sleep duty cycles to energy availability can increase throughput despite constrained resources [14]. In addition, passive voltage scaling (PVS) schemes eliminate costly DC-DC converters and increases efficiency from power delivery system to DC-DC converters by directly connecting the microprocessor with battery [17-18]. However, this puts a stringent requirement on the energy harvesting source supply voltage. In addition, the required

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maximum power point tracking task is much more complicated due to the removal of voltage regulators. A dynamic programming algorithm was also proposed for scheduling and operation of DVFS for heterogeneous voltage regulators, e.g. LDP or DC-DC converter in a battery energy source [19]. As voltage drops from the battery, different operation schemes are used to achieve optimal energy consumption. While the work lays out a solid framework for optimizing energy consumption under different types of regulators, two missing considerations limit the application of the work in our battery-less discussion, (1) the work cannot be directly transferred into an energy harvesting environment where source is volatile and MPP tracking is needed; (2) it does not utilize the more recent fully-integrated system where regulators are placed on the chip leading to significantly different energy profiles.

As a result, none of previous works address a fully-integrated system where power converters and management are integrated on the same chip as microprocessors. As will be shown in this paper, the conventional design strategy of optimal energy point or operation condition does not hold true in a fully integrated system. Hence, a new design optimization strategy must be established. Owing to the dynamic setting of energy harvesting condition, intelligent scheduling and management is needed at the system level. Co-optimization of power management, microprocessor, and energy harvesting is possible compared with traditional discrete modules. This paper provides a study and analysis, from a holistic point of view, on the battery-less energy harvesting system and proposes new solutions for maximizing power efficiency.

The contributions of this paper include: (1) a systematic optimization across all modules in a fully integrated SoC considering individual energy profiles. We show that up to 30% savings can be achieved with a holistic view of the system compared with conventional rule of thumb on individual models. (2) An intelligent scheduling and management method are proposed for MPP tracking and performance enhancement under dynamic change of environment leading to further improvement on system performance. (3) We demonstrate the proposed holistic energy optimization approach using solar energy harvesting system and a fully-integrated 65nm testchip.

II. Fully Integrated Energy Harvesting (EH) System

Fig. 1 shows the battery-less fully integrated energy harvesting system-on-chip (SoC). Instead of separate modules in conventional setup, the microprocessor directly interacts with integrated regulator to realize energy management, e.g. energy tracking. Such a system provides fast DVFS response, lower cost and global optimization as will be discussed in this paper. Since battery is replaced by a small capacitor, more complex circuitry such as boost converter, battery charger is eliminated in the system leading to low cost single chip solution ideal for IoT application. Voltage comparators can be used to perform MPP tracking as will be described in section VI.

A. Solar Cell Measurement and Operation Requirement

Efficient harvesting from photovoltaics is not straightforward, as the amount of energy harvested depends on the point voltage at the harvester, and the environmental conditions, e.g. full sunlight, indoor light, or cloudy. This relationship is represented by an I-V curve mapping harvesting current (I) to supply voltage (V). An off-shelf solar cell from IXYS (KX0B22-04X3F) is picked in this work, which delivers voltage and power suitable for our system power/voltage level while also avoiding high-ratio voltage conversion and boosting converter [20]. Fig. 2 shows experimental data gathered using the monocrystalline 22×7mm IXYS solar cell (22% conversion efficiency from light to energy) and a variable load. The solar cell was moved to different outdoor and indoor areas. The figure shows clearly that the I-V curve based on quantity of light (sunlight has more energy than indoor light).

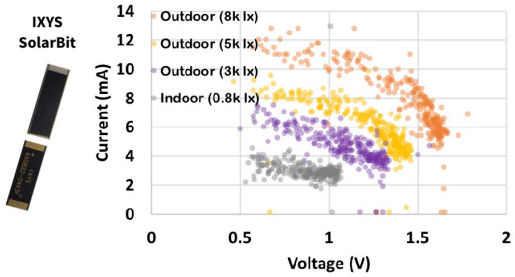


Fig. 2. Our measured solar cell I-V curve under variable condition.

III. Design And Energy Profile Of On-Chip Regulators

This section describes the typical on-chip fully-integrated regulators used for voltage generation and their energy profiles used in this work.

Linear regulator or low-dropout (LDO) regulators have the smallest area overhead and are most common. Fig. 3 shows the LDO schematic and its simulated efficiency implemented in this work at a 65nm CMOS process. The efficiency does not change significantly with load due to the resistive division.

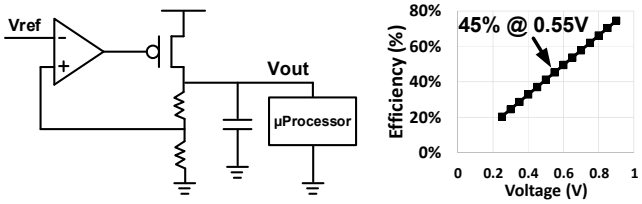


Fig. 3. LDO schematic and its efficiency in this work.

Switched-capacitor (SC) regulators have become a popular alternative to LDOs in recent years due to high efficiency. Fig. 4 shows the implemented SC regulator in this work and its efficiency. With full load (~10mW) at 0.55V, the power efficiency is 67%, which is significantly better than a linear regulator [7, 9]. SC regulator is common for low power application. However, due to the principle of operation, it is difficult to realize a large voltage range with high efficiency. As a result, multiple configurations must be used to cover large operating voltage range leading to overhead of the design [9].

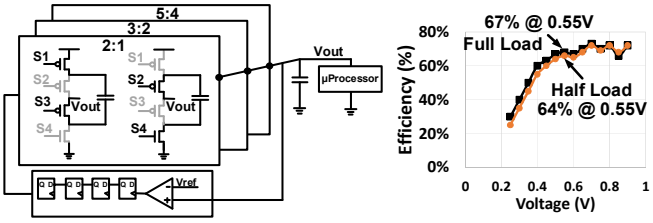


Fig. 4. SC regulator schematic and its efficiency in this work.

Buck regulators are another popular regulator commonly used for power management circuits. Although traditional buck regulator uses off-chip inductors, strong interest has been drawn in recent years on designing highly efficient on-chip buck regulator which uses integrated on-chip inductors. Fig. 5 shows the implemented buck regulator and its efficiency. Compared with SC regulator, buck regulator performs better at high output power but shows equal or less efficiency at low output power [21-23].

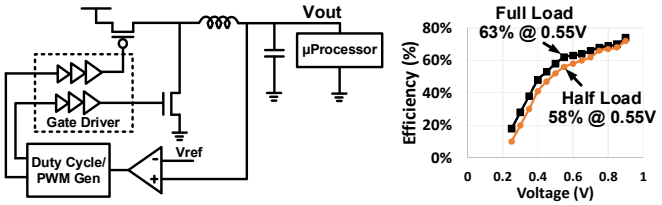


Fig. 5. Buck regulator schematic and its efficiency in this work.

IV. Optimal Voltage Point For Performance

In this section, we formulate the design strategy for optimizing performance under energy constraint from solar cell considering fully-integrated power management system.

A. Optimal Voltage Point of Microprocessor

While substantial existing work provides circuit techniques for tracking the maximum power point (MPP) from solar energy harvesters, there is a lack of consideration in energy management literature considering internal circuits, e.g. microprocessor. We show that it is critical to take a holistic look at the entire system rather than previous module level design strategy which only renders local optimization. Equations (1-4) formulates the problem statement.

$$Maximize\ f_{clk} \quad (1)$$

Subject to:

Max Power Source Constraint:

$$P_{\mu P} = \eta(V_{dd}) \cdot P_{MPP\_Solar} \quad (2)$$

Max Speed Constraint:

$$f_{clk} \leq f_{max}(V_{dd}) \quad (3)$$

And power relationship:

$$P_{\mu P} \propto C{V_{dd}}^2 f_{clk} + P_{leak} \quad (4)$$

where P_{MPP_Solar} is the maximum power point of solar cell, η is the efficiency of integrated regulator at a particular supply voltage.

Modern regulators typically have a MPP tracking circuit to dynamically adjust power loading to the solar cell so that the operating voltage stays near MPP. In a fully integrated system, as the digital microprocessor directly interacts with voltage regulators, the dynamic load can be adaptively tuned by adjusting clock f_{clk} and supply voltage V_{dd} to the microprocessor. As a result, a feedback system is established from regulator down to microprocessor through digital processor core to maintain the solar cell operating at the maximum harvesting state. According to equations (1) to (4), the entire system has to satisfy the incoming power constraint from solar cell while trying to optimize its performance, i.e. clock speed.

Fig. 6(a) shows the simulated power consumption of our test vehicle, i.e. an image processor (refer to section VII), across voltages at its maximum speed. The power curve of solar cell is also shown. Without voltage regulator, the microprocessor operates at the intersection of the solar I-V curve and its own power-V_{dd} curve leading to a significantly reduced incoming power source. The use of voltage regulator allows maximum power to be extracted even when the microprocessor operates at lower voltage than MPP of solar cell. However, the efficiency loss of on-chip regulator compromises its gain leading to degraded power utilization rate. As shown in Fig. 6(b), with the example of SC regulator running in out-door strong light condition, the use of on-chip voltage regulator allows 31% more power to be extracted and leads to 18% speedup. The benefit of using buck regulator is slightly less than that from SC regulator due to a reduced efficiency. The LDO does not bring any efficiency improvement over raw solar cell because the additional available power extracted from the solar cell is proportionally lost due to the efficiency loss from LDO which linearly scales with output voltage. In fact, overall, less power is delivered from the LDO due to additional power consumption of LDO. This observation highlights the importance of budgeting regulator efficiency in overall operation of microprocessor and harvester, which has been typically ignored in previous study.

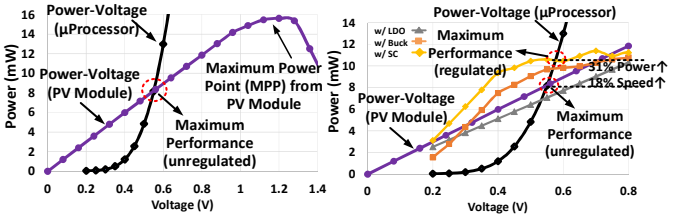


Fig. 6. (a) Power from solar cell and microprocessor, and (b) regulated output power from various types of regulators.

B. Optimization under Low Light Condition

In energy harvesting environments, the light source can undergo significant variation. We observe that the benefit of on-chip regulator reduces when operating at low light condition where low power from microprocessor reduces the regulator efficiency. As a result, the saving from operating solar cell at MPP is offset by the loss of energy through low efficiency of regulator. Fig. 7(a) shows the simulated savings from on-chip SC regulator under different light condition. While 30~40% more power is achieved at 100% and 50% of solar output, under 25%, the output power from regulator becomes ~20% less than delivered from a raw solar cell due to regulator inefficiency at low load. Hence, bypassing the regulator and operating from the solar cells under low light operation is best.

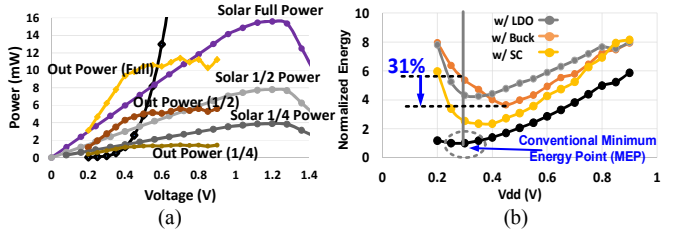


Fig. 7. (a) Output power from regulators under variable light condition, and (b) minimum energy point (MEP) in a fully-integrated system versus conventional MEP.

V. Optimal Energy Point For Energy Reservation

The above analysis assumes the scenario that all energy resources are allocated to the microprocessor. If a full system operates under capacitor/battery manager and other processing units, a minimum energy point (MEP) is often desirable from the microprocessor to minimize its energy consumption for other resources assuming performance is not a constraint [24]. Under such a condition, operating the system at MEP is critical and the optimization equation from (1) to (4) is changed to below:

$$\text{Minimize E} = \eta(V_{dd}) \cdot (E_{dyn} + \text{E}_{leak}) \quad (5)$$

$$\textit{Subject to } E_{dyn} \propto CV_{dd}{}^2 \text{ and}$$

$$E_{leak} \propto P_{leak}(V_{dd})/f_{clk}(V_{dd})$$

where E_{dyn} is dynamic energy consumption and is only related to the supply voltage V_{dd} while E_{leak} is leakage of the microprocessor and is a function of leakage power and clock speed, both of which are functions of V_{dd}.

The equation (5) is similar to conventional definition of MEP for a microprocessor except that the energy efficiency of voltage regulator has to be considered [24]. As efficiency of voltage regulator is also a function of supply voltage, the overall MEP is different from what is considered in conventional design. We performed an analysis on our test image processor with measured dynamic and leakage power consumption. Fig. 7(b) shows the results in comparison to conventional MEP for microprocessor operation versus the fully-integrated system where various voltage regulators are utilized. The minimum energy voltage is shifted higher than conventional method with SC and buck regulator cases by up to 0.1V leading to up to 31% energy reduction compared with using conventional MEP. The difference is due to the change of energy efficiency from different voltage regulator profiles. The inefficiency of voltage regulators offset the energy reduction at very low voltage leading to higher minimum voltage point. Such an effect has not been considered previously and becomes important in energy harvesting environments where the voltage regulator is used to maximize energy generation.

VI. Scheduling Considerations: Time And Energy

A. MPP Tracking under Dynamic Energy Change

Power consumption can be directly managed through the operation of the microprocessor using a DVFS scheme for MPP tracking. Challenges emerge from sudden input source changes, such as light dimmed due to an obstacle. We propose a simple scheme that utilizes the capacitor discharge time for extraction of the in-situ IV curve for MPP tracking. Compared to current measurement [18], the proposed technique can be done faster and is easily derived without additional circuitry or software. Fig. 8 shows the proposed scheme and simulated waveform from Cadence Virtuoso. Real-time input power can be derived by tracking the time that voltage drops across a predefined threshold. A look-up table is used to map the measured power to corresponding MPP point, so that DVFS is adjusted to operate around the new MPP point when significant energy source changes occur. Shown in Fig. 8, assuming dramatic change of input power leads to solar voltage change from V_1 to V_2, power and total voltage change at output of solar cell is given by:

$$P_{in} \cdot t + 1/2(CV_1^2 - CV_2^2) = P_{out} \cdot t/\eta \quad (6)$$

where P_{in} is input power and solar cell, P_{out} is output power of the regulator, which is a known function of voltage and clock speed of the microprocessor, C is the capacitor at output of solar cell, η is the efficiency of regulators, V_1 and V_2 are comparator threshold voltages that monitors the solar panel output and t is the time that output traverse from V_1 to V_2. The input power of the solar cell can be derived from how long it takes to trigger comparators threshold voltages from V_1 to V_2:

$$P_{in} = \frac{P_{out}}{\eta} - \frac{(CV_1^2 - CV_2^2)}{2 \cdot t} \quad (7)$$

The obtained P_{in} can be used to select predefined energy profile as well as MPP voltage leading to a simple way of performing MPP track under dynamic condition of solar cell.

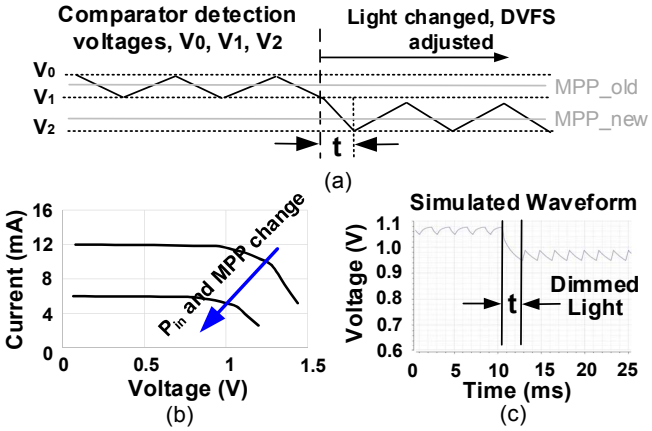


Fig. 8. Proposed MPP tracking using time tracking from threshold crossing. (a) Illustration of operation scheme, (b) simulated I-V curve and (c) solar output voltage.

B. Optimal Schedule under Timing Constraint

The analysis in section V, was set for a steady state operation where the microprocessor consumes the maximum power offered from a solar harvester. In existing applications, the operation is often constrained by completion time. Under such circumstances, the microprocessor has to operate beyond the maximum power to meet the deadline. To allow the completion of task under tight timing constraint, capacitor is used to temporarily supply extra energy used for operation. The operation is completed before input voltage from capacitor is dropped too low to halt the operation of the microprocessor. Large duty cycle is used to restore the voltage on the capacitor after the operation.

The required energy from the source for a microprocessor is given below:

$$E_{out} = N/\eta \cdot \alpha \cdot V_{dd}^2 \quad (8)$$

where N is the total number of clock cycles. α is lumped parameter to account for capacitance of internal circuit. η is the efficiency of the regulator.

The total operation time is:

$$T = N/f_{clk} \cong N/(\beta \cdot V_{dd}^{\theta}) \quad (9)$$

where β and θ models the frequency as a function of V_{dd}. Assuming frequency is close to a linear function of V_{dd},

$$E_{out} \cong \frac{\alpha N^3}{\eta \beta^2 T} \quad (10)$$

Equation (10) models the energy required from the source to achieve a desired completion time. The input energy comes from both solar cell and capacitor:

$$E_{in} = E_{cap} + E_{solar} \quad (11)$$

where $E_{cap} = \frac{1}{2}CV_{start}^2 - \frac{1}{2}CV_{end}^2 \cong constant$

$$E_{solar} = \int_0^T P_{solar} dt \cong I_{in} \cdot (V_{start} - V_{end})/2 \cdot T$$

Fig. 9(a) shows energy trend versus completion time for incoming energy and output energy. To push for faster completion time, higher incoming energy is needed. The resulted completion time is when the two curves intersect. Note that supply voltage and speed of the microprocessor is kept constant through voltage regulator which, in the case of switching regulator, can be assumed to have relatively constant efficiency η over the operation range.

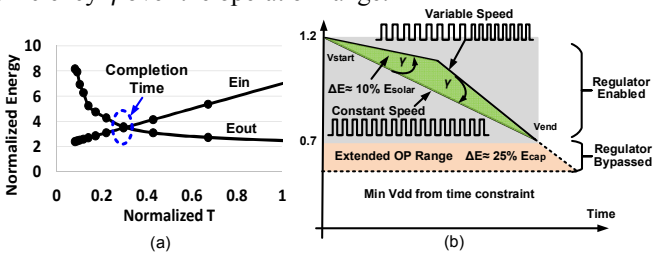


Fig. 9. Proposed sprinting operation. (a) Completion time versus energy consumption from solar input and microprocessor, and (b) illustration of sprinting operation and bypass operation of regulator.

To optimize the energy consumption under the timely operation situation, we propose a "sprinting" operation where variable speed of microprocessor is utilized to maximize the energy intake from the solar cell. Fig. 9(b) shows the proposed "sprinting" operation. As the energy efficiency from switching regulators remain relatively constant for a range of voltages, we vary the energy consumption from microprocessor to allow more time for solar panel to operate at higher voltage such that more energy is extracted from light source. As voltage drops, the microprocessor starts to sprint to achieve the required completion time. The voltage curve compared with normal operation is shown. The area under the voltage traverse curve represents the gained energy from solar source which can be converted into microprocessor operation speed. The extra energy saving can be calculated as below assuming a sprinting factor of γ which represents the percentage of slowing down or speeding up at beginning and later of the operation. For simplicity, we assume at the first half of the operation, the operation slows down while the second half speeds up. The extra energy taken from solar cell is:

$$\Delta E \cong \int_{t_{start}}^{t_{end}} I_{in} V(t) dt = 2\gamma \cdot (V_{start} - V_{end})/2 \cdot T \quad (12)$$

The extra energy absorbed is given by:

$$\varepsilon = \frac{\Delta E}{E} \cong \frac{2\gamma(V_{start} - V_{end})}{V_{start} + V_{end}} \quad (13)$$

To further improve the efficiency from harvesting system, we combine the "sprinting" operation with bypassing voltage regulator operation. This allows energy to be delivered to microprocessor before the voltage in the system becomes too low to sustain timely operation. Fig. 9(b) shows combining the "sprinting" operation and regulator bypass increases solar cell energy delivery under strict timing constraint up to 25%.

VII. System Demonstration

Fig. 10 shows a chip configuration and test board for our measurement. The 4mm^2 65nm testchip consists of fully-integrated buck regulator which operates from 0.3 to 0.8V under 1.2 to 1.5V supply with efficiency 40%~75% across voltage and loading condition as shown in Fig. 5. It also includes a pattern recognition image processor which performs feature extraction and classification by using gradient feature vectors in a windowed frame. Image pixels are externally scanned into chip and stored in on-chip memory. For a low resolution image with 64×64 pixels, it takes about 15ms to process at 0.5V. The quarter sized test PCB consists of a single solar panel as described in Section II. To facilitate V_{dd} tracking, multiple comparators with less than 0.1μW power are added on the board to serve as a simplified energy monitor to the solar cells. The comparators feedback digitalized results to the clock generator and voltage regulator of the SoC chip to modulate the speed of processor and voltage of the regulator.

Fig. 11(a) shows the measured speed and energy contributors, i.e. leakage, dynamic energy from microprocessor and regulator. Fig. 11(b) shows the measured waveform of the proposed operation in section VI. As the light dims, solar V_{dd} starts to decay due to the loss of energy source. However, the voltage regulator sustains the output voltage between 0.6V to 0.5V to allow completion of the job on time. Controlled by energy tracking comparators, between 1.2 to 0.9V, the processor ran at slower speed. As the solar voltage dropped below 0.9V, the processor accelerated the speed until the regulator was not able to sustain the voltage at output above 0.5V. At that point, the regulator was bypassed allowing the solar cell to directly charge up the processor supply so that the operation of was extended. As shown in the measured waveforms of the operation, the operation was extended by 3ms or 20% from the bypassing operation and 10% more energy was absorbed from solar cell by sprinting operation at 20% rate.

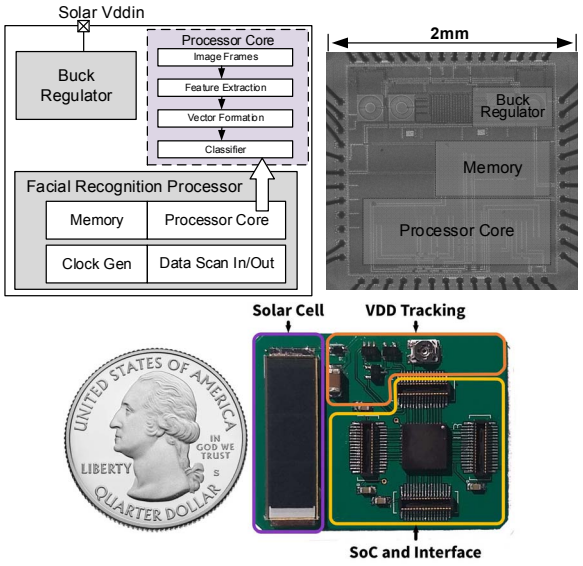
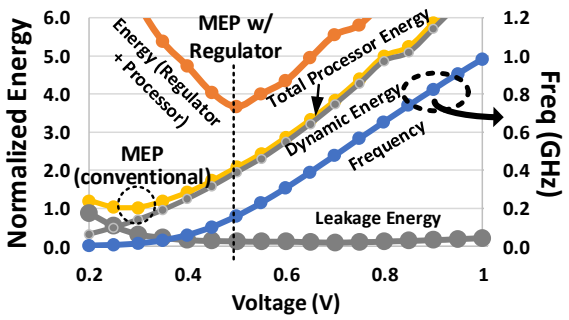
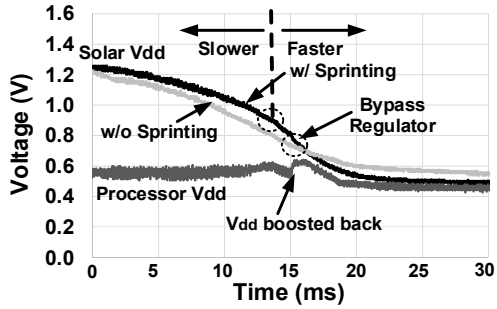


Fig. 10. Schematic and die photo of the test chip and the test PCB.



(a)



(b)

Fig. 11. (a) Measured system characteristics, speed and energy/power, and (b) measured waveform of the proposed sprinting operation.

VIII. Conclusions

There is a lack of systematic optimization considering both power management, harvesting and microprocessors. This paper shows a holistic study on the energy management of battery-less energy harvesting system. We show that the optimal operation voltage and minimum energy point are different from conventional design strategy when considering the energy/power profile of each module. Up to 30% energy savings could be achieved when performing a holistic modeling and optimization. We develop a MPP tracking and scheduling scheme, leading to up to 20% boost of the available energy from the energy harvesting system. We demonstrated the holistic analysis and operation scheme in a battery-less energy harvesting system with fully-integrated testchip.

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